REMARKS

Claims 1-21 are rejected under 35 USC §102(a) as being unpatentable over Fitzgerald et al., U.S. PCT WO 02/15244A2.

Independent claim 1 recites a method of bonding lattice-mismatched semiconductors. The method includes forming a Ge-based virtual substrate and depositing on the virtual substrate a CMP layer which is polished to form a planarized virtual substrate. Also, the method includes bonding a Si substrate to the planarized virtual substrate and performing layer exfoliation on selective layers of the planarized virtual substrate producing a damaged layer of Ge. Furthermore, the method includes removing the damaged layer of Ge.

Independent claim 12 recites a method of bonding lattice-mismatched semiconductors. The method includes forming a Ge-based virtual substrate, using the virtual substrate is used to form a planarized virtual substrate, and bonding a Si substrate to the planarized virtual substrate. Furthermore, the method includes removing selective layers of damaged Ge of the planarized virtual substrate associated with the Ge-based virtual substrate.

Fitzgerald et al. '244 describes a process for producing monocrystalline semiconductor layers. With respect to claim 1 and 12, Fitzgerald et al '244 does mention the use of Ge-based virtual substrates, but does not teach or suggest performing layer exfoliation on selective layers of the planarized virtual substrate producing a damaged layer of Ge or removing selective layers of damaged Ge of the planarized virtual substrate associated with the Ge-based virtual substrate. Furthermore, Fitzgerald et al. '244 describes a deposited oxide layer as it pertains

to creating an electrically passive interface. There is no discussion of using this layer to facilitate planarization of a Ge virtual substrate prior to wafer bonding.

In particular, Fitzgerald et al '244 describes a SiGe layer being transferred on top of 550 nm buried oxide, thus showing surface damage. Moreover, Fitzgerald et al '244 describes using annealing to split and remove a relaxed $Si_{1-y}Ge_y$ layer. There is no discussion of a damaged Ge layer or removal of the damaged layer by a self-limiting, i.e. selective etch in Fitzgerald et al. '244. Thus, claims 1 and 12 are not anticipated by Fitzgerald et al '244.

As to claims 4 and 10-17, they are dependent on claim 1, respectively. Therefore, claims 4, and 4 and 10-17 are also allowable for the same reasons argued with respect to claim 1.

In view of the above amendments and for all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the rejections made under 35 U.S.C. §102. Accordingly, an early indication of allowability is earnestly solicited.

If the Examiner has any questions regarding matters pending in this application, please feel free to contact the undersigned below.

Respectfully submitted,

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